AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes changes to Fig. 10. This sheet, which includes Fig. 10, replaces the original sheet including Fig. 10. In particular, Fig. 10 has been labeled "prior art."

REMARKS

This is in response to the Office Action dated October 31, 2006. Claims 1-17 are currently pending.

Fig. 10 has been labeled "prior art" as requested by the Examiner. However, Figs. 11-12 are not prior art, and thus have not been labeled as such.

The specification has been amended as requested by the Examiner. Thus, the formality objections have been addressed and resolved.

Claims 1-2

Claims 1-2 stand rejected under Section 103(a) as being allegedly unpatentable over alleged admitted prior art in view of Kazunari. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

The alleged admitted prior art (APA) is not prior art. The description set forth in the instant specification at page 5, lines 10-21, relied on by the Examiner, is *not* "prior art." Thus, it will be appreciated that the problem recited from page 5, line 22 to page 7, line 7, of the instant specification is not prior art to the instant application. Because these features/problem are not prior art, they cannot be relied on in a Section 103(a) rejection. Thus, the Section 103(a) rejection is fundamentally flawed as being based on non-prior art material, and should be withdrawn. Claims 1-2 are in condition for allowance.

Other Claims

Furthermore, with respect to claim 8, there is no teaching or suggestion in any art cited by the Examiner of providing a wiring load adjustment section *using a liquid crystal layer as a dielectric for equalizing the wiring load of the first and second signals.*

With respect to claim 9, there is no teaching or suggestion in any art cited by the Examiner of providing the dummy wiring in a *fanfold shape in an area closer to an end portion of the substrate than the data signal line driving circuit.*

With respect to claim 11, there is no teaching or suggestion in any art cited by the Examiner of making such a dummy wiring in a periphery of a display section of the device.

With respect to claim 12, there is no teaching or suggestion in any art cited by the Examiner of *using an interlayer insulation film of the display as a dielectric for equalizing the wiring load of the first and second signals.*

With respect to claim 13 (and 15), there is no teaching or suggestion in any art cited by the Examiner of providing such a dummy wiring in a periphery of a display section of the device.

With respect to claim 14, there is no teaching or suggestion in any art cited by the Examiner of *using a gate insulation film of a TFT as a dielectric for equalizing the wiring load of the first and second signals.*

Conclusion

It is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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By: _____

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